UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/508,802	09/23/2004	Tomohisa Shiga	450100-04421	3919

7590 10/01/2008

William S Frommer
Frommer Lawrence & Haug
745 Fifth Avenue
New York, NY 10151

EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
10/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/508,802	SHIGA, TOMOHISA	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,14-16 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,14-16 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/28/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 27 August 2008 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5, 14-16 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal et al. (U.S. Patent No. 5,890,222) herein referred to as Agarwal.

3. Regarding claim 1 and 14, Agarwal discloses an operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising: a register array having a plurality of registers (Register File 238; see Fig. 3) each for holding an arbitrary value based on a write address and a write control signal (see col. 6, lines 18-20) and for outputting the held value to a signal line (inherently, any output must be sent on a signal line) based on a read address (General Purpose Register Address 342, see Fig. 5); an operation portion having an input coupled to said signal line (selected via the General Purpose Register Address 342; see col. 2, lines 39-42) independent of an intervening addressable register (the address is gathered from indirect register 330, which is directly used to select the target register; see fig. 5) such that a value read from said register array to said signal line based on a read address (General Purpose Register Address) is capable of being provided to said input without further addressing (The General Purpose Register Address selects the output register) a register, the operation portion being operable for performing an operation on said value read from said register array to said signal line (based on the OP Code; see Fig. 4; col. 6, last 4 lines); an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion (inherently, a computer system executing instructions must decode the instructions), wherein said operation instruction includes at least one bit indicative of an access method (Indirect Access Bit 312; see Figs 4 and 5); and an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion (Control Unit 130; see Fig. 2,

col. 4, lines 37-42), wherein, in the event said at least one bit is indicative of a first access method, then said instruction-execution-controlling portion is operable for (i) selecting one of said registers based on said operation instruction (Selection Bits; see Fig. 6), and (ii) based on a value held by said selected register, performing register-to-register addressing processing for selecting another of said registers of said register array (Using the General Purpose Register Address; see above; also see col. 8, lines 20-30): and wherein, in the event said at least one bit is indicative of a second access method, then said instruction-execution-controlling portion is operable for selecting one of said registers based on said operation instruction (Operand Field; See Fig. 6), and not performing register-to-register addressing processing for selecting, based on a value held by said selected register, another of said registers of said register array (See col. 8, lines 37-42).

4. Regarding claim 3 and 16, Agarwal further discloses said operation program includes an operation instruction to perform the register-to-register address processing (the system is designed specifically to perform register-to-register addressing, therefore an instruction would exist in the programs run on the machine).

5. Regarding claims 5 and 16, Agarwal further discloses that said instruction execution-controlling portion has: a first selector for selecting any one of a read execution address (A Operand 306; see Fig. 4; col. 7, lines 4-12) a to select said one register and a read address to select this register again (the same address; if used in a

next instruction, it will still select the same register); and a second selector for selecting any one of a write execution address (Target Operand 304; see Fig. 4; col. 7, lines 4-12) to select said one register and a write address to select this register again (the same address).

6. Regarding claim 26, Agarwal further discloses at least one input signal line that is coupled to said signal line via a latch (inherently if dataflow is controlled by a clock, data is stored in latches and therefore every data source is latched).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal in view of Shimanek et al. (U.S. Patent No. 7,023,744) herein referred to as Shimanek.

Regarding claims 2 and 4, Agarwal does not expressly disclose a program stored on a read only memory wherein said register array and the read only memory are each

comprised of a plurality of memory cells wherein said operation portion, the instruction–decoding portion, and the instruction-execution-controlling portion are comprised of a plurality of arithmetic/logic operation elements and wherein said memory cells and the arithmetic/logic operation elements comprise a programmable logic device and are formed on an identical semiconductor chip.

Shimanek teaches storing information on a ROM (Non-volatile memory 120; see Fig. 1) in the identical semiconductor chip (chip 100; see Fig. 1) as logic implanted in a plurality of arithmetic/logic operation elements (Configurable logic and interconnect 105; see Fig. 1) to form a programmable logic device.

It would have been obvious for one of ordinary skill in the art to have modified the invention of Agarwal by implementing the program on a read only memory and the operation portion, the instruction–decoding portion, and the instruction-execution-controlling portion on a plurality of Arithmetic/Logic operation elements to for a single chip PLD, as taught by Shimanek, in order to decrease the design time by using a PLD and decrease costs by using a single chip.

Response to Arguments

9. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

/J. R. M./
Examiner, Art Unit 2181

/Niketa I. Patel/
Primary Examiner, Art Unit 2181